Application for United States Letters Patent

for

Differential Metal Oxide Semiconductor Capacitor

by

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Field

Embodiments of the present invention relate to circuits, and more particularly, to capacitors.

Background

Metal Oxide Semiconductor (MOS) capacitors are needed in many analog integrated circuit applications requiring high capacitor density. A common approach to realizing a MOS capacitor is shown in Fig. 1. In Fig. 1, nMOSFET (n-Metal Oxide Semiconductor Field Effect Transistor) **102** has source **104** and drain **106** shorted to ground (substrate) **108** to form one plate of a capacitor, and gate **110** serves as the other plate.

In many applications, there is a need for a high density capacitor using a digital CMOS (Complementary Metal Oxide Semiconductor) process in which the voltage difference between the terminals of the capacitor are small. For example, Fig. 2 illustrates operational amplifier (OPAMP) **202**, which is part of some larger circuit **222**, such as, for example, an analog-to-digital converter, or a communication circuit such as an Ethernet PHY. OPAMP **202** comprises first differential stage **204** and a final output stage comprising nMOSFET **206** biased by current source **210**, where the output signal is taken at output port **212** and input signals are applied at input ports **214** and **216**. Miller compensation is applied to nMOSFET **206** by connecting capacitor **208** as shown in Fig. 2. Other stages, employing nMOSFETs, pMOSFETs, or both types of transistors, may be present in OPAMP **202**, but for simplicity are not shown. The voltage difference between terminals **218** and **220** of capacitor **208** may be small, such as much less than 0.1 volts.

Operating capacitor **102** in its linear range usually requires a voltage difference across its terminals equal to or greater than its threshold voltage. For many process technologies, this threshold voltage is on the order of 0.7 volts. Even for process technologies where native MOS devices are available, the threshold voltage may still be about 0.1 to 0.2 volts. Consequently, using the structure of capacitor **102** in Fig. 1 for capacitor **208** in Fig. 2 may not be suitable.

Brief Description of the Drawings

Fig. 1 is a prior art floating MOS capacitor.

Fig. 2 is a prior art Miller-compensated operational amplifier.

Fig. 3 is a capacitor according to an embodiment of the present invention utilizing nMOSFETs.

Fig. 4 is a capacitor according to an embodiment of the present invention utilizing pMOSFETs.

Fig. 5 is a capacitor according to an embodiment of the present invention utilizing nMOSFETs and a npn transistor.

Fig. 6 is a capacitor according to an embodiment of the present invention utilizing pMOSFETs and a pnp transistor.

Description of Embodiments

Fig. 3 illustrates an embodiment of the present invention, where the source and drains of nMOSFETs **302** and **304** are connected to each other, and are connected to the drain of nMOSFET **306**. nMOSFET **306** has its gate connected to its drain, and has its source connected to ground (substrate potential). Gates **308** and **310** of nMOSFETs **302** and **304** comprise the two terminals of the resulting capacitor.

Because in normal operation DC (Direct Current) is not conducted via gates **308** and **310**, the DC bias current through nMOSFET **306** is zero. Consequently, the gate-to-source potential difference of nMOSFET **306** is zero, and nMOSFET **306** is OFF. As a result, the circuit of Fig. 3 does not consume DC power, and the impedance between gates **308** and **310** is capacitive.

The potential difference between gates **308** and **310** need not necessarily be at the threshold voltage of the nMOSFETs in order for the channels of pMOSFETs **302** and **304** to be in inversion. This is observed by noting that when the gate-to-source potential difference for both nMOSFETs **302** and **304** equals the threshold voltage, the potential difference between gates **308** and **310** is zero. For the Miller compensated output stage of OPAMP **202** in Fig. 2, the gate potential of nMOSFET **206** and the output potential of output port **212** may both be about 0.9 volts, and consequently the embodiment capacitor of Fig. 3 may be used for capacitor **208** of Fig. 2 because 0.9 volts is higher that than the threshold voltage for may typical nMOS devices.

Other embodiments may utilize pMOSFETs rather than nMOSFETs. For example, in Fig. 4, pMOSFETs **402** and **404** have their sources and drains connected to each other and to the drain of pMOSFET **406**, where the gate and drain of pMOSFET

406 are connected to each other. Gates **408** and **410** comprise the two terminals of the resulting capacitor. In other embodiments, bias transistor **306** or bias transistor **406** may be realized by a bipolar transistor. For example, in Fig. 5, nMOSFETs **502** and **504** have their sources and drains connected to the collector of npn transistor **506**, where the base and collector of npn transistor **506** are connected to each other. Gates **506** and **508** comprise the terminals of the resulting capacitor. As another example, in Fig. 6 pMOSFETs **602** and **604** have their sources and drains connected to the collector of pnp transistor **606**, where the base and collector of pnp transistor **606** are connected to each other. Gates **608** and **610** comprise the terminals of the resulting capacitor. Accordingly, variations and modifications to the disclosed embodiments may be realized without departing from the scope of the invention as claimed below.